What is claimed is:

1. A high availability telecom/datacom architecture comprising:

dual/redundant ethernet switches;

a plurality of I/O cards connected to the dual/redundant ethernet switches; and

at least two CPUs coupled to each other and to the plurality of I/O cards via the ethernet switches.

2. The architecture of claim 1 further comprising:

a system monitor and control module coupled to the at least two CPUs and the plurality of I/O cards via the ethernet switches.

3. A high availability telecom/datacom architecture comprising:

dual/redundant network links;

a plurality of I/O cards connected to the dual/redundant network links; and

a system controller coupled to the plurality of I/O cards via the dual/redundant network links.

4. The architecture of claim 3 wherein the system controller comprises multiple CPUs coupled to each other and to the plurality of I/O cards via the dual/redundant network links.

5. The architecture of claim 3 wherein the dual/redundant network links are implemented using ethernet switches.

6. The architecture of claim 4 wherein the dual/redundant network links are implemented using ethernet switches.

7. The architecture of claim 3 further comprising:

a system monitor and control module coupled to the system controller and the plurality of I/O cards via the network links.

8. The architecture of claim 5 further comprising:

a system monitor and control module coupled to the system controller and the plurality of I/O cards via the network links.

9. A network bus architecture for providing high availability to telecom/datacom systems comprising:

dual/redundant network links;

a plurality of I/O cards connected to the dual/redundant network links; and,

a system controller coupled to each other and to the plurality of I/O cards via the dual/redundant network links.

10. The network bus architecture of claim 9 wherein the network links are implemented using ethernet switches.

11. The architecture of claim 10 wherein the system controller comprises multiple CPUs coupled to each other and to the plurality of I/O cards via the ethernet switches.

12. The architecture of claim 9 wherein the system controller comprises multiple CPUs coupled to each other and to the plurality of I/O cards via the network links.

13. The architecture of claim 9 further comprising:

a system monitor and control node coupled to the system controller and the plurality of I/O cards.

14. The architecture of claim 12 further comprising:

a system monitor and control node coupled to the system controller and the plurality of I/O cards.

15. The architecture of claim 9 further comprising software and APIs.